Low-Noise MESFET's for Ion-Implanted GaAs MMIC's

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Abstract—**Fabrication considerations for low-noise FET's in ion-implanted GaAs monolithic microwave integrated circuits (MMIC's) are presented. Processes that can deteriorate FET performance have been identified and some solutions proposed. Low-noise MMIC FET's fabricated along these lines show good microwave performance through 18 GHz, approaching the performance available from similar discrete FET's. 0.8-μm gate-length MMIC FET's with a noise figure of 2.9 dB and associated gain of 6.1 dB at 18 GHz have been fabricated. These devices are suitable for low-noise applications in ion-implanted GaAs MMIC's.**

I. Introduction

GALLIUM ARSENIDE monolithic microwave integrated circuit (MMIC) technology has matured rapidly during the last few years. MMIC's reported in the literature reflect increasing levels of chip complexity and a wide range of microwave applications [1]–[3]. One of the areas of interest at the present time is the improvement of yield through a better control of fabrication processes and an understanding of the effect of each fabrication step on device performance. In this paper, the performance of low-noise MMIC FET's is discussed.

We have reported [4] an ion-implantation-based process for the fabrication of GaAs MMIC's incorporating active devices, RF and dc biasing circuitry, and bypass capacitors. The process involves multiple, localized ion implantation in qualified semi-insulating GaAs substrates for active-layer formation, contact photolithography for patterning, plasma-enhanced CVD silicon nitride for metal–insulator–metal (MIM) capacitors, and a two-level metallization scheme with air bridge crossovers. Via holes through the substrate are etched as necessary for providing a low-inductance connection to the ground plane on the back of the wafer. Discrete FET's (from test patterns) fabricated by this ten-mask-level process have been compared with standard FET's fabricated in our laboratory using an abbreviated process consisting of only four mask levels. Both types of FET's (Fig. 1), have $\sim 0.8\text{-}\mu\text{m} \times 300\text{-}\mu\text{m}$ refractory metal-based gates. Initial results indicated that the FET's obtained from the complete MMIC process had higher noise figures and lower gains than the standard FET's. The differences were attributed to the extra processing seen by the MMIC FET's, and a study was initiated to identify the causes for FET degradation. The results of this study are presented below.

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II. Device Fabrication

The MMIC fabrication process described in [4] is outlined schematically in Fig. 2. As shown there, FET fabrication is complete at the end of step no. 3. The remaining processes are required to fabricate the other components (MIM capacitors, RF and dc circuitry, via holes, etc.) comprising an MMIC. In addition to a reactively sputtered silicon nitride cap for annealing implant damage (not shown in Fig. 2), two other silicon nitride layers are used in the fabrication process. Both of these layers are deposited at 250°C by plasma-enhanced CVD. The first silicon nitride layer (deposited after ohmic contact alloying) is used for dielectric-aided liftoff [5] of FET gates and the first metallization level, which forms ohmic contact overlays, and the bottom electrode of MIM capacitors. Experience has shown that this technique results in a straightforward high yield process. The second dielectric layer is used for MIM capacitors.

Discrete FET's are also fabricated in our laboratory. Essentially the same process is used, except implantation over the entire wafer, in conjunction with mesa etching, is used to define active layers rather than localized implantation, and front-end processing is terminated at the end of step no. 3 in Fig. 2. Patterning of the gate metallization by direct liftoff (without the use of nitride) is preferred for discrete FET's, since it allows fabrication of gates with shorter gate lengths than is possible by dielectric-aided liftoff.

III. Process-Device Interactions

The performance of MMIC FET's differs from that of discrete FET's due to the additional processing steps required in MMIC fabrication. Important changes in FET characteristics can occur due to the following:

1) ohmic contact degradation during thermal cycles associated with dielectric deposition,

2) damage or etching of exposed active layers (especially between gate and source) during plasma processes, e.g., dielectric deposition and reactive ion etching, and

3) increased gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitance due to a layer of high-dielectric constant material (e.g., silicon nitride) over the FET.

Ohmic contact degradation was observed in the first generation MMIC's fabricated in our laboratory which used the same process that was then being used for low-noise FET's. This consisted of *e*-beam evaporation of Au

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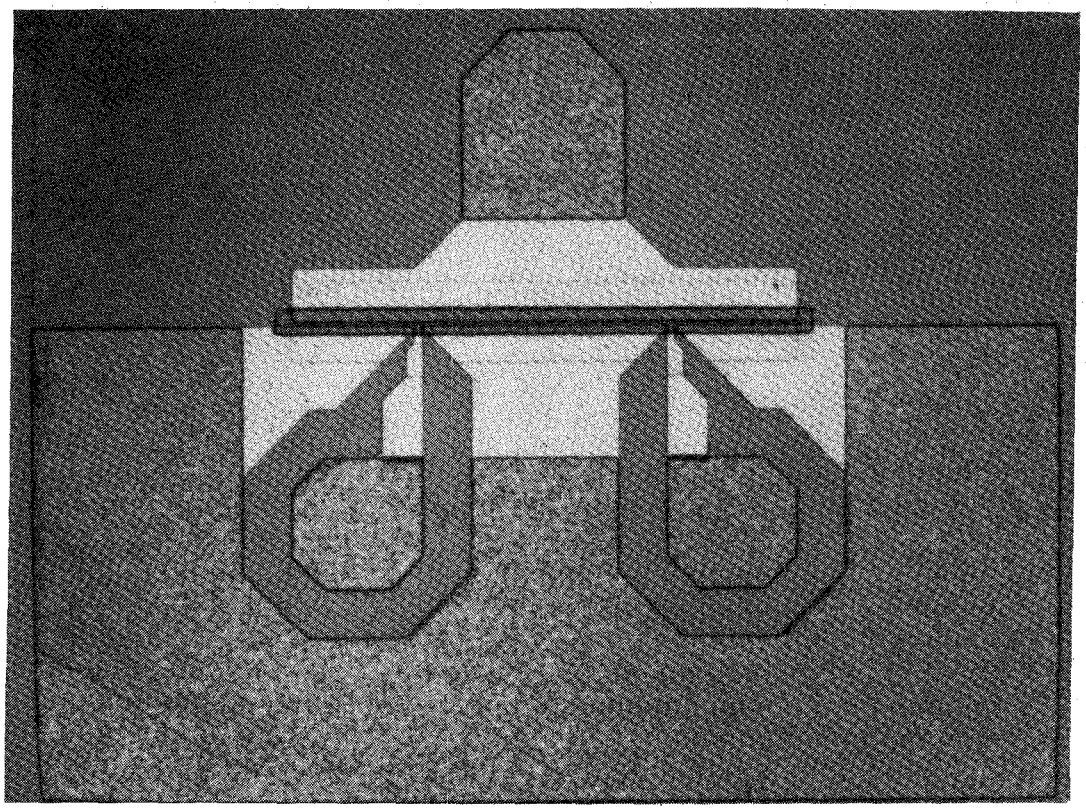

Fig. 1. Photograph of the discrete low-noise MMIC FET used for evaluation. Gate dimensions are ~ 0.8 μm × 300 μm.

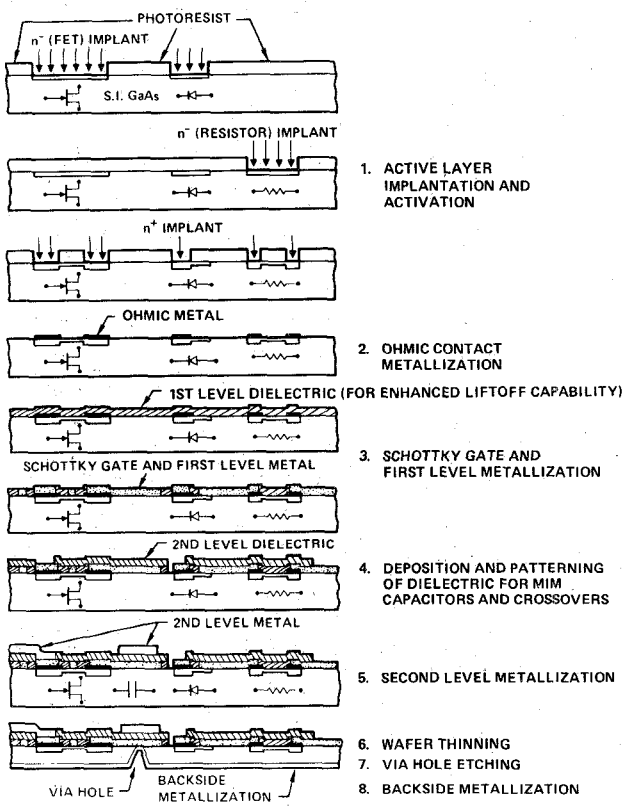

Fig. 2. A schematic outline of the MMIC fabrication process.

(88 wt%)–Ge (12 wt%) and Pt on a lightly etched GaAs surface, patterning by liftoff, and alloying at 450°C for 60 s in forming gas. Typically, this resulted in a specific

TABLE I
SPECIFIC CONTACT RESISTANCE RESULTS

Metallization: AuGe/Pt	
Wafer No.	R_c (micro-ohm cm^2)
144	50.8
165	9.06
173	25.4
174	8.54

Specific ohmic contact resistance measured after completion of all MMIC fabrication steps. Note the large variation. Typically, $R_c \leq 3\times10^{-6}$ $\Omega\cdot$cm^2 is observed immediately after sintering the contacts.

contact resistance of ~ 1–3×10^{-6} $\Omega\cdot$cm^2. When ohmic contact resistance was measured again after the completion of all subsequent MMIC steps, an increase was always observed as shown in Table I for some representative wafers. In order to identify the reasons for contact degradation, specific contact resistance was measured on AuGe/Pt- and AuGe/Ni-based contacts (with and without an overlay) as a function of isochronal annealing on several test wafers. The results are shown in Fig. 3. The test samples were heated for 30 min in air at 150, 250, and 350°C each and contact resistance was measured after each cycle. The results clearly indicate that both contact systems, without an overlay, remain stable through the heating cycles, but AuGe/Pt contacts with Ti(500 Å)–Pt(1000 Å)–Au(3500 Å) overlay degrade when subjected to heating cycles. Thus, it appears that the contact resistance on MMIC wafers increased during the two nitride deposition steps which subject the wafers to 250°C for ~ 30 min. Fig. 3 also shows that AuGe/Ni-based contacts

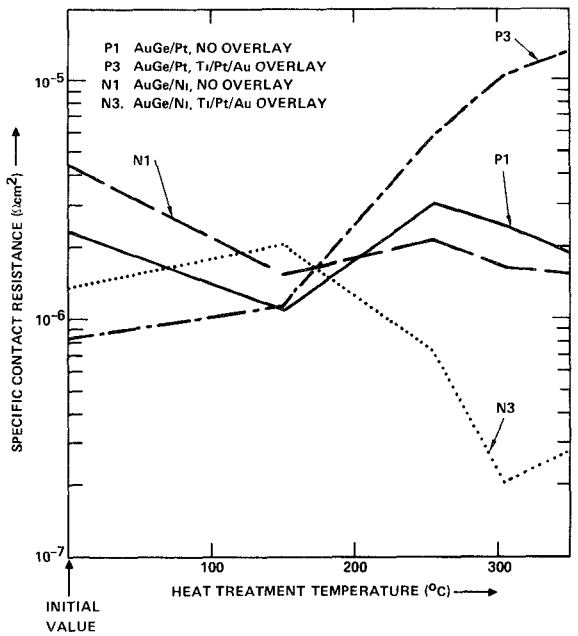

Fig. 3. Specific contact resistance as a function of isochronal annealing for AuGe/Pt- and AuGe/Ni-based contacts. The wafers were heated for 30 min in air at 150, 250, and 350 °C each, and contact resistance was measured after each heating cycle.

are free of this problem. Therefore, AuGe/Pt contacts were replaced by AuGe/Ni contacts, and low ohmic contact resistance has since been observed as shown by the data in [4].

The atomic mechanism responsible for this phenomenon is not understood at the present time. However, these data are in agreement with those of Lee *et al.* [6] who studied the long-term reliability of AuGe/Pt and AuGe/Ni ohmic contacts to GaAs and concluded that "AuGe/Pt contacts are stable without overlay but degrade rapidly with overlay."

The problem of inadvertently damaging or etching exposed active layers is quite serious. This is most likely to happen during processes in which the wafer is subjected to ion bombardment (e.g., ion milling, reactive ion etching, dielectric deposition by plasma-enhanced CVD, etc.) or wet chemical etching. When this happens, the sheet resistance of the layer increases and, in the case of the FET, increases the parasitic gate-to-source resistance, thereby increasing noise figure of the device. To illustrate the magnitude of this effect, a GaAs wafer with a silicon-implanted active layer (125 keV, 3.5×10^{12} cm^{-2}) was prepared for FET fabrication by mesa etching and by forming ohmic contacts. Sheet resistance of the layer and I_{dss} (before gate) of 200-μm-wide FET's were measured across the wafer. A 5000-Å silicon nitride layer was then deposited by plasma-enhanced CVD. Substrate temperature was kept at 250 °C and a 13.56-MHz RF power (inductively coupled) of 100 W was used. Next, via holes were etched in the nitride to access the ohmic pads, and the previous measurements were repeated. The results (Table II) show that the damage to the layer is substantial. The product $\rho_\square \times I_{dss}$ is approximately constant as expected. It

TABLE II
EFFECT OF ION BOMBARDMENT ON ACTIVE LAYERS

	Before Dielectric Deposition	After Dielectric Deposition
Average Sheet Resistance ($\rho_\square$)	769.0 Ω/□	1089.0 Ω/□
Average I_{DSS} (before gate) w = 200 μm	80.2 mA	59.5 mA
$\rho_\square \times I_{DSS}$	61.7 V	64.8 V

has been found in the past that sometimes it is possible to anneal this surface damage and restore original values of $\rho_\square$ and I_{dss} by heating the wafer to ~ 450 °C for 1–2 min. However, metallization systems always degraded significantly at such temperatures, and this was not considered a viable approach. Active-layer damage, as a function of power supply frequency for plasma-enhanced CVD deposition, was studied. A Technics PEII system, which uses a 30-KHz plasma generator, was used to deposit silicon nitride, and the above experiment was repeated. Although active-layer damage was reduced slightly (compared to Table II), it was still found to be unacceptably large.

This problem is especially serious for ion-implanted active layers, since these layers are generally much thinner than those that can be obtained by epitaxial techniques. Epitaxially grown FET layers can be made to have a sufficiently thick surface n^+ layer that can significantly reduce the effects of surface damage, such as that seen in plasma-enhanced CVD. However, due to a limitation of $\sim 2\times10^{18}$ cm^{-3} in the peak doping density that can be obtained by ion implnatation in conjunction with thermal annealing, and the fact that attempts to produce very deep ion-implanted layers result in a highly graded interface between the active layer and the substrate, which is unsuitable for low-noise applications, ion-implanted layers tend to be thin and hence more susceptible to damage by fabrication processes.

With recent developments in photo-CVD [7], it is now possible to deposit dielectric layers at low temperatures without the use of a plasma. This not only eliminates damage to the active layers (as observed in initial experiments), but it also allows liftoff techniques to be used with dielectric deposition since the deposition temperature can be kept below 100 °C.

When FET's are coated with a layer of high-dielectric-constant material like silicon nitride, both C_{gs} and C_{gd} increase. The exact change is difficult to measure accurately since the capacitances are very small in magnitude, however, preliminary measurements on a 300-μm-wide FET are summarized in Table III. Note that the increase in $C_{gs}+C_{gd}$ is approximately proportional to the dielectric constant of the protective coating. This change is especially significant for C_{gd}, which may increase by > 100 percent as a result of the dielectric. Previous attempts to etch off the dielectric over the FET's were not very satisfactory, due to the damage problem discussed earlier in this section. This problem can be alleviated by using direct liftoff for

TABLE III
EFFECT OF DIELECTRIC PASSIVATION ON VALUE OF C_{gs} AND C_{gd}

Dielectric	Approximate Dielectric Constant	Increase in $C_{gs} + C_{gd}$ for w = 300 μm
6000Å silicon nitride (deposited by plasma enhanced CVD)	7.3	50 fF
8800Å polyimide	3.5	26 fF

TABLE IV
SALIENT FEATURE OF MMIC LOW-NOISE FET'S

Active Layer:	Localized ion implantation through 500Å Si_3N_4; Si, 5E12, 100 keV and 5E12, 260 keV
Gate Length:	~ 0.8 μm W-Au (by contact photolithography)
Gate Width:	300 μm (4 × 75 μm)
Source-Drain Gap:	3.8 μm
Gate-Source Gap:	~ 0.9 μm

the FET gates and selective deposition of silicon nitride by photo-CVD only where needed, e.g., MIM capacitors, crossovers, etc. An alternate is to use a lower dielectric-constant film such as polyimide in place of the silicon nitride.

IV. MMIC FET PERFORMANCE

Discrete FET's (on test patterns) were fabricated by the complete MMIC process described earlier, except that changes were made to reflect the improvements outlined in the previous section. Direct liftoff was used for gate metallization and a 1.0-μm-thick layer of polyimide was used to protect the FET from plasma damage and to minimize the increase in C_{gs} and C_{gd}. The FET's were mounted in standard 70-mil low-noise FET packages for microwave evaluation. Similar discrete FET's fabricated by an abbreviated four-mask-level process were also packaged and tested for comparison. There was no scratch protection layer on these devices. The MMIC FET's had their source pads grounded through via holes, whereas the discrete FET's used multiple wire bonds to provide a low inductance source connection. Salient features of the MMIC FET's (Fig. 1) are summarized in Table IV. A comparison of the low-noise performance of discrete and MMIC FET's at 18 GHz is provided in Table V. The best minimum noise figure and associated gain of the discrete FET's is listed along with similar data for two representative MMIC wafers. Average minimum noise-figure values are within 0.3 dB of the best numbers. As shown by the data in Table V, the low-noise performance of MMIC FET's is comparable to the best published results for 0.8-μm gate-length GaAs FET's, making this device suitable for low-noise applications in monolithic circuits. The differences between discrete and MMIC FET's have also been minimized in spite of the additional processing steps for the MMIC FET's. With more experience, this difference is expected to be reduced even further.

TABLE V
BEST NOISE FIGURE AND ASSOCIATED GAIN DATA $f = 18$ GHz

Wafer No.	Type	Minimum Noise Figure (dB)	Associated Gain (dB)
A	Discrete	2.6	7.1
B	MMIC	2.9	6.1
C	MMIC	2.9	6.0

V. CONCLUSIONS

Fabrication considerations for low-noise FET's in ion-implanted GaAs MMIC's have been presented. In particular, processes that can deteriorate FET performance have been identified and some solutions proposed. Low-noise MMIC FET's fabricated along these lines show good microwave performance through 18 GHz, closely matching the performance available from discrete FET's and demonstrating that they are suitable for low-noise applications in ion-implanted GaAs MMIC's.

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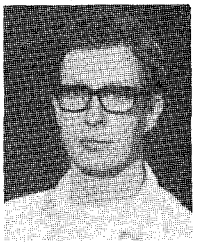

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